The above diagram describes our quality control procedure before releasing our designs to our foundry partner, Silterra. As all our designs i.e the GDS II files are transferred via the internet, a secured private FTP account, namely MyFab and MyFTP accounts are created by Silterra specifically for Key ASIC in order to ensure there are no unauthorised access to the database. At the same time, Silterra will provide their Foundry Service Manual and Standard Process Technology Design Support Documents via MyFab. Our design engineers will download all the fabrication device forms and latest process fabrication design rules and scripts from MyFab. This is to ensure that our design engineers are able to perform a final design verification using Silterra's provided rules and scripts with minimum design error. Once the design is completed, our design engineers will transfer the complete GDS II database to Silterra though the secure MyFTP account. Subsequently, Silterra will review and check the design database and the device forms to ensure that the fabrication process conform to quality standards and design specification. Once review is completed, Silterra will arrange the E-Jobview for Key ASIC. Our design engineers will then review the E-Jobview to ensure that the fabrication masking layers do not have any issue. Our design engineers will communicate their approval to Silterra via electronic mail to start mask writing process. Lastly, Silterra will kick-off the fabrication process.

(c) Design Back-up System

Apart from all the quality control procedures, in the event of any catastrophe like earthquake or fire, or business interruption due to the cut of electrical supply, our Group's internal design database is protected through an external design back-up system. Our internal design database is backed-up on a weekly basis to an off-site external storage.

5.4.7 Research and Development

(a) R&D Policy and Focus

We are committed to continuously carry out R&D efforts by keeping abreast with market developments and trends. We believe that continuous R&D is crucial in order to compete effectively.

Our Group conducts research in its core area of development such as commercialising silicon IPs, designing ASIC and SoC (including prototype) with high performance, low power consumption and small die size, developing turnkey services including back-end testing and fabrication manufacturing technology and verification. We base our engineering development using the following strategies:

(a) internal R&D utilising our own resources; and

(b) working in partnership with the leading players in different sectors, through design collaboration or joint ventures.

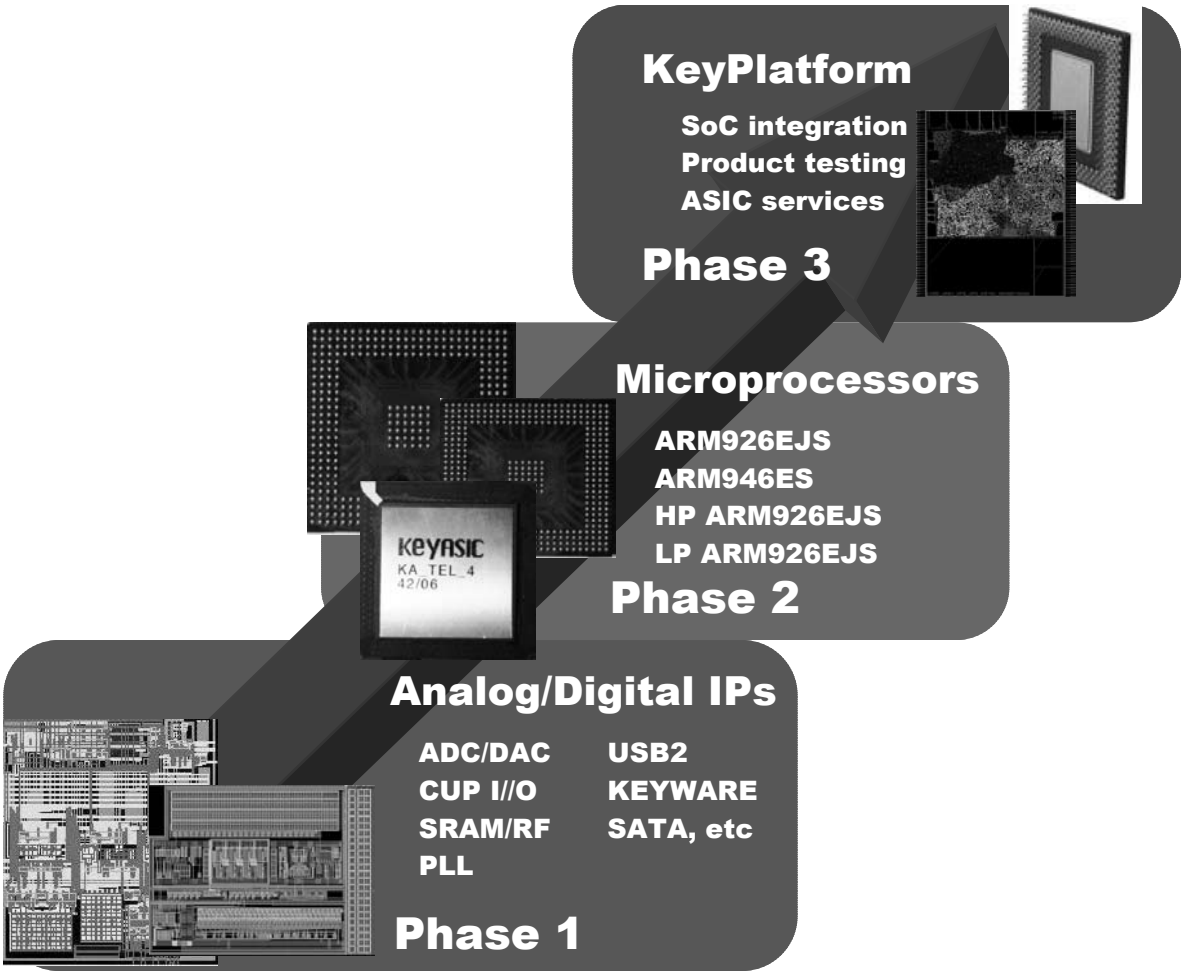

Figure 4: SoC development phases

Figure 4 above illustrates our R&D engineering development plan that comes in 3 phases. The first phase is to build the wireless and consumer end analogue and digital IPs, design and testing capabilities. The phase 2 development is to work on the high performance and low power consumption microprocessors that serve in the wireless and personal electronics segment. The phase 3 focus is to develop more SoC products such as VoIP, Wi-Fi, set-top box and MP3. The complete engineering competency development is planned across 3 years starting from 2006. Our main focus in the near term is to provide superior design flow and optimisation technology to quickly and cost-effectively meet SoC requirements for high-volume, high performance, and low cost consumer applications.

Our R&D engineering development roadmap is tightly mapped against Silterra's process roadmap. This is to ensure that we are able to provide design expertise and validate the new logic and mixed signal process technologies into Silterra. Currently, the technologies available under Silterra include various 0.18µ, 0.16µ and 0.13µ technologies. 0.11µ is currently under development and is scheduled to be available by first half of 2008.

(b) R&D Facilities and Technical Personnel

As an MSC status company, we have R&D offices located at Cyberjaya and Petaling Jaya. This Malaysian-based R&D facility will support its worldwide sales.

There are 16 designers who are involved in our R&D activities. The R&D engineering team is headed by Mr. Lai Kok Keong. Our R&D engineers have multiple years of design experience and some of them have worked with leading semiconductor companies around the world including but not limited to Intel Corporation, Agilent Technologies Ltd, Altera Corporation, Avago Technologies Ltd and National Semiconductor Sdn Bhd.

The design capabilities of our engineering team include the following:

- ASIC and SoC design experience for various technology nodes including but not limited to 0.25µ, 0.18µ, 0.16µ, 0.13µ, 0.11µ, 0.09µ and 0.065µ process technologies;
- High performance design including 3.0 GHz CPU in the past;
- Low power design for mobile and hand held devices such as cellular phones, MP3, PMP and hand-held games;
- CMOS and SOI technology design experience;
- Complete front to back design capability starting from specification, RTL, gate, layout to GDS II;
- Advanced design methodology including ASIC design flow, semi-custom and custom design flow; and
- Ability to design all IPs in the SoC including CPU, Memory, I/O and Analogue.

Our management plans to expand the R&D team in the next 2 years. The total number of R&D staff is expected to increase to 45 personnel by the FYE 2009.

FYE	2007	2008	2009
Total R&D staff	16	34	45

(c) Investment in R&D

We did not incur any R&D cost during the year of our incorporation in 2005. However in the FYE 2006 and the 9-month FPE 2007, our total investments in R&D were RM2.07 million and RM2.44 million respectively which representing about 4.1% and 8.5% of our total turnover for the same year/period. We have budgeted an annual R&D expenditure of approximately 24% of our annual consolidated revenue from the FYE 2008 up to the FYE 2009, to finance our R&D activities.

We will continue to invest heavily in our R&D activities and have allocated RM36 million from our listing proceeds towards R&D. Please refer to Section 3.8 of this Prospectus for further information on the proceeds used for R&D activities.

(d) R&D Milestones

2006: Our engineers' main focus was improving Key ASIC design flow, circuit optimisation technology and enriching our analogue IPs. Our R&D team has developed a set of analogue IPs and general CPU based on various 0.18µ, 0.16µ and 0.13µ technologies. Our ARM 926/946 CPUs developed are characterised both in Silterra's 0.18µ and 0.13µ process technology. A number of consumer and electronic applications have also been developed for customers namely, MP3, DVD, PMP Wi-Fi, WiMAX and VoIP. We have also developed a design flow that will automate the shrinking process.

2007: Our R&D engineers will continue to focus on porting IPs and plan to complete porting of all defined IPs on Silterra's 0.13µ technology. Our R&D engineers have developed a prototype high performance ARM926 CPU at 333MHz on Silterra's 0.13µ technology as compared to the ordinary ARM926 CPU at 250MHz. We will focus our engineering expertise on CMOS 0.16µ, 0.13µ, 0.11µ and low power process and will work closely with Silterra to develop and fine tune the 0.11µ device model in line with Silterra's 0.11µ roadmap.

2008: New IPs development focus will be on 0.11µ and 0.09µ process technologies. In addition, our Group will also expand our application platforms and will also be developing some new IP needs. We will also work on low power CPU, KeyWare, low power custom memory and optimising circuit techniques to provide customers with complete low power solutions.

2009: We will work closely with Silterra to develop the 0.065µ test chip and fine tune the fabrication process and device modelling. Developing a new methodology to support the use of multiple cores in a single SoC will also be necessary. Design for manufacturing will be one of our future focuses that we are looking into incorporating into our design flow.

5.4.8 Competitive Strengths and Advantages

We believe that our competitive strengths and advantages lie in the ability of our technical team to design high performance, low power consumption and smaller size chips which includes CPU, DSP and graphic design.

Our strengths in the above areas are, to a large extent, achieved through the following:

(i) Experienced management team and strong technical personnel

Our Group consists of an experienced management team coupled with an experienced Board of Directors who have helped define the product roadmap for the development of new chip design ideas for ASIC and SoC. Our management team and Board of Directors have many years of design experience at some of the world's leading semiconductor companies which includes Intel Corporation, Agilent Technologies Ltd, Synopsys Inc., Altera Corporation, Avago Technologies Ltd and National Semiconductor Sdn Bhd. As a result, our Group is able to leverage on the wide network of our experienced management team. Please refer to Sections 7.1 and 7.3 for more details on our Director's and key management profile.

One distinct competitive advantage that our Group possesses over other design companies is that our technical personnel has the technical expertise in the system architecture design and RTL to netlist design, and the ability to optimise the design to maximise the performance, reduce power and die size at a cheaper cost. Most design service companies provide place and route service, and are not capable of providing architecture level and RTL to netlist design service. Our experienced team of designers has consistently delivered many high performance CPUs, DSP and graphics designs and many communication and consumer SoC. High performance and low power is the core competency of our design team.

(ii) Strong strategic partnership with foundry players

In Malaysia, there are only 2 process foundries, namely X-FAB Sarawak Sdn Bhd *(formerly known as 1st Silicon (Malaysia) Sdn Bhd)* and Silterra. Silterra is a growing process foundry service provider. It offers CMOS logic, high voltage and mixed-signal/radio frequency process technologies to customers of all sizes worldwide including many top-tier semiconductor companies. Silterra is the first foundry partner to our Group as we have a complete set of IPs and design capability targeting products that are suitable for Silterra's process technologies. This is also an important partnership to the foundry as the foundry would require chips designed into its foundry process technologies so that they can get wafer manufacturing business. Our Group has developed and ported our IPs on Silterra's 0.18µ, 0.16µ and 0.13µ technologies. At the same time, we have outsourced our manufacturing process to Silterra.

Having formed a strong strategic partnership with Silterra, our Group is able to provide customers with a more complete solution by having a one-stop design-to-manufacture service as compared to many advanced players in Malaysia. Our Group has preferential access to Silterra's foundry capacity which guarantees us short turn around time and on-time delivery, even for small to moderate volumes.

(iii) Rich set of IP portfolio

Our Group currently has more than 50 different peripheral IPs developed and ported that are silicon proven, targeting the consumer electronics and communication segment. Through our KeyIP Service, our Group offers customers the ability to license IPs from our pool of mixed-signal and digital IP, including interfaces, IPs blocks, CPU and DSP cores. Our Group has developed a complete set of IPs for platform of VoIP, Wi-Fi, MP3, DVD, set top box, image processor, multimedia server and PMP. The key differentiator of our Group is the ability to develop a set of datapath IP components such as various arithmetic integer adders, barrier shifters, incrementer and decrementer for optimisation of speed, power and die size of the ASIC and SoC. For instance, KeyWare is a set of various IP blocks developed by our Group optimised for performance and power.

(iv) Possess high-end SoC designs

A SoC design incorporates a whole system on a single chip, containing CPU processors, embedded memory, peripherals, and other system blocks. Combining SoC modules with various design styles on a single chip will dramatically increase the complexity of the following areas:

- Die size reduction
- Functional verification
- Power reduction
- Physical verification
- Performance improvement

Yet, as complexity increases, the time to get these devices to market continues to decrease.

Producing these highly complex SoC designs requires an experienced design team to employ highly efficient design methodology and high end SoC modules (CPUs, embedded memory peripherals, etc) to overcome the issues that arise in the above mentioned areas.

Our Group is able to provide smaller die size, lower power and higher performance SoC modules such as CPU and other peripheral IPs to develop the complex SoC designs. Furthermore, the engineering group is experienced in EDA design methodology development that is able to reduce the design time and design iterations.

(v) Ability to design high-end CPU for consumer electronics

Our Group is one of the few IC design service companies in the world that possesses high end CPU, DSP, memory design experience and capability. Currently, we have developed high performance ARM946E-S CPU which is based on ARM architecture that is capable of operating at 200MHz internal clock speed, which is 18% faster than the original ARM946E-S that normally operates at 170MHz. On the power consumption part, we are able to achieve approximately 7% lower at 0.84uW/MHz than the original ARM946E-S which was running at 0.90 uW/MHz. CPU/DSP and memory is the critical part of any SoC. With the continuous push for performance, low power consumption and smaller die size, optimisation of CPU speed and reduction of power becomes a unique competitive edge that we possess as compared to many design houses in the world.

(vi) One-stop solution service centre

Our Group offers our customers a single point of contact for our high-end SoC integration starting from high-level marketing specifications down to tape-out to a foundry to fully qualify ASIC and SoC products. Our Group handles the whole design chain and adds key value to the stages of the development to ensure successful delivery of the end product. With the strategic partnerships of our foundry partners and testing houses, we are able to handle all intermediate stages of the design efficiently and ensure the overall performance and quality of the SoC is maintained. This has definitely provided us with a more complete solution to customers than most advanced players.

5.4.9 Key Milestones, Awards and Recognition

Month / Year	Major events
August 2005	Incorporation of Key ASIC in Malaysia
November 2005	Formed partnership with Silterra
March 2006	Developed and ported our first set of IPs on the 0.18µ process technology of Silterra
April 2006	Announced our design-to-manufacture services for portable and consumer applications Granted MSC status by MdeC
May 2006	Successfully tape-out high performance, low power consumption ARM946E-S CPU
September 2006	Developed and ported our first set of IP on the 0.13µ process technology of Silterra
December 2006	Delivered the 0.13µ PDK validation to Silterra
February 2007	Tape-out SkyMedi products
June 2007	Incorporation of KASSB

Month / Year	Major events
July 2007	Tape-out Gigabit Ethernet product that has smaller die size and faster speed. Proven high speed and low power techniques in customer product.
August 2007	Successfully delivered the Silterra C13G CUP I/O IPs
September 2007	Post-silicon verified 0.13u ARM946E-S 30% better performance than standard specifications. ARM946E-S operates at 270MHz
October 2007	Completed the Silterra CL130G PDK validation. Tape-out customer from USA (Intellasys) Place & Route project within 7 days.

5.4.10 Interruptions to Business

We did not experience any disruption in our business which has a significant effect on our operations for the 12 months period prior to the date of this Prospectus.

5.4.11 Intellectual Properties

Save as disclosed below, we do not own any other registered brand names, trademarks or licenses:

(i) Copyright of all our peripherals IPs; and

(ii) License over our peripherals IPs and EDA tools

5.4.12 Principal Place of Business

The principal place of business of our Group as well as our core R&D personnel and activities are located at Lot 6.03, Level 6, KPMG Tower, No. 8 First Avenue, Bandar Utama, 47800 Petaling Jaya, Selangor Darul Ehsan and Unit No.: C207, 2nd Floor, Block No. 3440 (Enterprise Building 1) Cyberjaya respectively.

5.5 MAJOR SUPPLIERS

Our major suppliers for the past 2 FYE 2006 and the 9-month FPE 2007 which contributes 10% or more of our Group's total purchases are set out below:

Supplier	Country	Length of relationship	<---------% of purchases --------> FYE 2005	FYE 2006	FPE 2007
KAL	Taiwan	Since September 2005	-	66.05%	17.74%
Key ASIC Inc	USA	Since January 2006	-	33.95%	61.90%
Global Grand Group Ltd	Taiwan	Since October 2006	-	-	16.05%

We are, to a certain extent, dependent on our current suppliers for provision of EDA design tools as well as the development, design and licensing of certain IPs. We have entered into Software License Agreement and Technology License Agreement with KAL whereby we were granted non-exclusive rights to install the software and to use or authorize use of the software and to use certain technology provided by KAL. Pursuant to the Outsourcing Agreement with KAL, KAL shall assists in developing, design and licensing certain IPs to us. We have also entered into an Outsourcing Agreement with KA Inc. whereby we are licensed to use certain ported IPs of KA Inc. These agreements were entered into as we have limited resources to develop and design certain IPs required in view that we were then only a start-up company. Further, it is also very expensive to develop our own EDA tools internally.

Outsourcing is an industry norm in the semiconductor industry due to the high capital and labour cost involved and increasing competition which drive companies to reduce costs and shorten time-to-market. Also, our industry entails high expertise to operate and the lack of competitive local IC design support as well as lack of IC design talent both in quantity and experience, has prompted us to outsource our design facilities to overseas expertise. It is also part of our business strategy to adopt the outsourcing model as and when required.

Going forward, the outsourcing of IP development and design is expected to decline as the basic IPs required for design engagement have been substantially developed in the FYE 2006 and most of these IPs can be re-used for many years. This is because the algorithm design of these IPs do not change in principle. Nevertheless, we may outsource certain IP development and design to third parties as and when the need arises and ensure that the arrangements are in the best interest of our Group. Meanwhile, we will continue to recruit experienced and technical personnel. We have also taken continuous efforts to strengthen and enhance our relationships with our existing outsourcing partners and also build new relationships. This would provide us a wider range of outsourcing facilities and hence, ensure that our operations continue to run smoothly.

5.6 MAJOR CUSTOMERS

Our major customers for the past 2 FYE 2006 and 9-month FPE 2007 which contributes 10% or more of our Group's total revenue are set out below:

Customer	Country	Length of relationship	<--------% of revenue --------> FYE 2005	FYE 2006	FPE 2007
Silterra	Malaysia	Since March 2006	-	87.32%	84.16%
Global Grand Group Ltd	Taiwan	Since October 2006	-	11.53%	-
MTek Limited	Taiwan	Since September 2007	-	-	12.30%

Our Group is, to a certain extent, dependent on Silterra as about 84% of our Group's revenue for the 9-month FPE 2007 is from sales to Silterra, of which 76% revenue from licensing and porting of IP designed specifically for Silterra's semiconductor manufacturing process technology and 8% revenue from commission earned for introducing about half of the end customers to Silterra. Silterra is a process foundry in Malaysia. However, due to the nature of the semiconductor industry, it is a norm for pure IC design houses to form strategic partnership with foundries and subcontract its manufacturing work to pure foundries. As we have the ability to have our technology designed specifically into Silterra's process technologies and as a result of that, Silterra can get wafer manufacturing business, this can be seen as an inter-dependent relationship that can be beneficial to both parties. This tight collaboration between ASIC design service companies and the foundries can be seen in successful business models such as Faraday Technology Corporation, a design service company listed in Taipei Stock Exchange collaborating with United Microelectronics Corporation, a world leading semiconductor foundry in Taiwan, as well as Global Unichip Corporation, the second largest ASIC design service company collaborating with its major shareholder, TSMC, a leading foundry player, both located in Taiwan.

Emulating these successful business models, we have signed a Foundry Service Sales Representative Agreement with Silterra, whereby we are appointed as marketing representative for Silterra in certain countries, and we will be paid a commission for acquiring the sale of silicon wafers fabricated by Silterra. We have also entered into IP Porting Services Agreement and CPU Agreement with Silterra, whereby we shall provide design services and license of IP to Silterra whilst Silterra shall undertake to manufacture the chips designed by our Group containing the ported IP using only manufacturing process specified in such agreements.

Please refer to Sections 4.2.7 and 5.4.1 for additional information on the relationship between Silterra and the Group.

5. INFORMATION ON OUR GROUP *(CONT'D)*

5.7 FUTURE PLANS, STRATEGIES AND GROWTH PROSPECTS

Our Group's mission is to provide customers with SoC platforms of various applications to reduce the design time and enable first time silicon success. Wireless, high performance and low power consumption is the key to our future IC designs. We aspire to maintain our position as the leading IC designer in Malaysia. To this end, we will build on our current strengths and competitive advantages and further explore new opportunities for market expansion. In this regard, the action plan put in place by us to ensure continuing business growth includes the following:

5.7.1 R&D Engineering Development Plan

Our engineering development roadmap is tightly mapped against Silterra's process roadmap. This is to ensure that we are able to provide the design expertise and validate the new logic and mixed signal process technologies into Silterra. Figure 5 below illustrates the technology roadmap of Silterra.

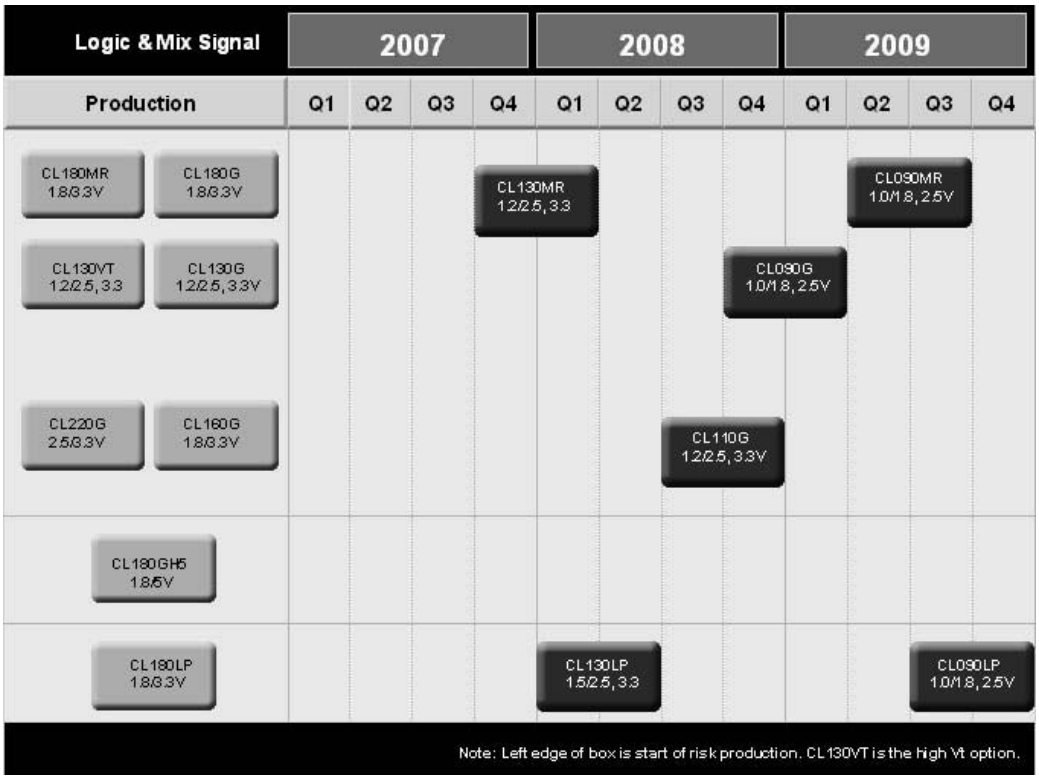

Figure 5 – Silterra's process technology roadmap

Currently, the technologies available under Silterra include various 0.18µ, 0.16µ and 0.13µ technologies. 0.11µ and 0.09µ technologies are currently under development and are scheduled to be available in 2008. The above diagram shows that the process technology is shrinking in size. We have mapped our R&D engineering roadmap into Silterra's process roadmap as illustrated in Figure 6 below. In the near term, our plan is to provide superior design flow and optimisation technology to quickly and cost-effectively meet SoC requirements for high volume, high performance and low cost consumer applications.

In 2007, our R&D engineers' main focus is to improve the ASIC design flow and to improve product testing and characterisation. We will continue to focus on porting IPs and plan to complete porting of all defined IPs on Silterra's 0.13µ technology. Our R&D engineers are also working on designing a higher performance ARM926 CPU at a higher speed of 333MHz on Silterra's 0.13µ technology as compared to the ordinary base performance ARM926 CPU at a speed of 250MHz. Programmable I/O and CUP I/O are also in the midst of being developed currently. Our engineers will work closely with Silterra to improve the process by using TSMC's process as a benchmark.

In 2008, our engineering design techniques will focus on porting and characterising existing IP's into Silterra's 0.11µ and 0.09µ technologies depending on Silterra's process availability. We intend to work closely with Silterra to develop the 0.11µ and 0.09µ test chips and fine tune the fabrication process by using other foundries' process as a benchmark. In addition, our Group will also expand our application platforms and will also be developing more specific IP application needs.

	2006	2007	2008
0.065G			✓ General CPUs for consumer end and mobile products in different foundry
0.09G /LP	✓ Specific analog IPs for the consumer end and mobile products.	✓ More specific analog IPs for the consumer end and mobile products.	✓ More specific analog IPs for the consumer end and mobile products.
0.13MVT /LP	✓ Design service (ASIC) ✓ High performance CPU for consumer end and mobile products	✓ Design service (SoC, ASIC) ✓ High performance CPU for consumer end and mobile products	✓ Design service (RTL coding & validation, SoC, ASIC) ✓ Low Power CPU for consumer end and mobile products
0.13HVT	✓ High performance (HP) KEYWARE development	✓ More HP KEYWARE development	✓ Low power KEYWARE development
0.13G	✓ Product testing and packaging capability ✓ COT process migration procedures	✓ Product testing and packaging capability ✓ KeyPlatform development	✓ SoC Product testing and packaging capability ✓ KeyPlatform enhancement
0.16LP	✓ Target process (Silterra) o 0.18G o 0.16G o 0.16LP o 0.13G o 0.13HVT	✓ Target process (Silterra/TSMC) o 0.16LP o 0.16G o 0.13G o 0.13HVT o 0.09G	✓ Target process (Silterra/TSMC/SMIC) o 0.13G o 0.13MVT/LP o 0.09G o 0.065G
0.16G			
0.18G			

Figure 6 – R&D Engineering Development Plan

5.8 LANDED PROPERTY

The landed properties rented by our Group are as follows:

Postal address	Owner/ Management Company	Existing use	Land/ Built-up area sq ft	#CF	Rental payable per month RM	Duration of tenancy
Lot 6.03 KPMG Tower No. 8, First Avenue Bandar Utama 47800 Petaling Jaya Selangor Darul Ehsan	Bandar Utama City Sdn Bhd (Company No. 268323-H)	Corporate office	6,813 square feet	Issued on 17.07.06	25,889	3 years (commencing from 1 July 2007)
Unit No.: C207, 2nd Floor, Block No. 3440 (Enterprise Building 1) Cyberjaya	Setia Haruman Sdn Bhd (Company No. 425154-U)	Corporate Office	1,133 square feet	Issued on 19.08.02	3,059	2 years (commencing from 1 September 2007) with an option to renew for a further 1 year

Notes:

 # CF represents certificate of fitness for occupation.

As far as our Directors are aware, there has been no material non-compliance with any laws, rules and building regulations in relation to the use of the above properties rented by our Group.

We do not own any property and we have not acquired any property since the date of our incorporation up to and including the date of this Prospectus.

6. INDUSTRY OVERVIEW

6.1 OVERVIEW

6.1.1 Overview of the Malaysian Economy

Malaysia's 50 years of nationhood marks another milestone in its economic development. Upon independence, the nation was highly reliant on tin and rubber and more than half of the population were in poverty. Today, Malaysia is a broad-based and diversified economy. The Government's far-sighted and pro-business policies were instrumental in the transformation of the economy. Towards this goal, economic management in 2007 is focused on enhancing domestic resilience to facilitate growth and development as envisaged in the National Mission, which commits to continuing the structural transformation towards becoming a developed nation by 2020. In this context, initiatives were taken to liberalise the Foreign Investment Committee guidelines, reduce corporate tax to 26% in 2008 through special incentives, strengthening of the human capital development and improving the public transportation and delivery systems.

With these measures and initiatives, all sectors of the economy will continue to expand. In an environment of low inflation and unemployment, high savings, favourable exchange rate as well as strong current account balance, the macroeconomic fundamentals of the country remain strong. The Malaysian economy is expected to expand strongly by 6.0% in 2007. The services sector, with an anticipated of 9.0% will continue to be the major contibutor to real GDP on the back of robust activities in intermediate services comprising finance and insurance, real estate and business services, transport and storage as well as the communications industry. The manufacturing sector is expected to pick up gradually and expand by 3.1%, following the anticipated recovery in global electronics demand in the second half. On the demand side, growth will be driven by resilient public and private sector expenditure, flowing stronger consumer sentiment, business confidence and higher Government spending. Nominal gross national product is estimated to increase by 9.4% to RM607,212 million, with per capita income increasing by 7.2% to RM22,345 (2006: 9.9%; RM20,841). In terms of Purchasing Power Parity ("PPP"), per capita income is expected to increase by 13.9% to reach USD13,289 in 2007 (2006: 13.0%; USD11,663).

The Malaysian economy is expected to register robust growth in 2008, with real GDP expanding between 6.0% and 6.5%. This translates to a 6.8% growth in nominal per capita income, rising from RM22,345 in 2007 to RM23,864 in 2008 or in PPP terms from USD13,289 to USD14,206. With an unemployment rate of 3.3%, the Malaysian economy will continue to operate under full employment. In tandem with the Government's efforts to ensure fiscal sustainability, the fiscal deficit will continue to decline to 3.1% of GDP. Malaysia's balance of payments position is expected to remain strong with the current account recording a surplus for the 11th consecutive year. The current account surplus amounting to 13.0% of GDP will emanate from the goods and travels account.

(Source: Economic Report 2007/2008)

6.1.2 Overview and Outlook of the World Economy

The global economy is expected to continue expanding for the 5th consecutive year in 2007, albeit at a more moderate pace, amidst high crude oil prices and uncertainties in the economy of the USA. While growth is relatively lower than the 2006 performance, it is nonetheless expected to remain strong with further expansion in economic activities especially in fast-growing emerging economies, notably China, India and Russia as well as recovering Europe and Japan. Global inflation remains at manageable levels although it has edged upwards due to high crude oil prices.

For advanced countries, growth is more balanced across regions with the steady recovery in Europe and Japan partially offsetting the moderation in the USA. Developing countries, primarily driven by investment and robust trade, are expected to outperform advanced countries and increasingly contribute to global growth. In this context, China, India and Russia are anticipated to account for more than half of this year's growth. Rapid growth has also led several developing countries to significantly contribute to outward foreign direct investment ("FDI"), an area where traditionally, developed countries were the main sources.

The more widely-spread growth in 2007 is expected to spill over into 2008, with world trade and investment projected to continue steadily expanding, and against a backdrop of relatively benign inflation. The favourable environment is expected to contribute positively to the Malaysian economy. In addition, Malaysia's continued engagement in regional and multilateral cooperation is set to further deepen its integration with the global economy.

Global growth in 2008, expected to be generally more-broad based both across regions and within countries, will continue to spur world trade and investment flows. Growth in world trade volume is projected at 7.4% in 2008 (2007:7.1%) supported by steady demand-driven expansion in global-high technology industries, commodities and services. With regard to investment, global FDI is expected to remain strong, driven by rising merger and acquisition activities, sustained economic growth and an increase in fixed capital spending. Leading FDI recipients among the developed countries would be the USA, Belgium, Luxembourg, France and the United Kingdom while China, Hong Kong SAR, Singapore and India are expected to be the top four among the newly industrialised and emerging economies.

(Source: Economic Report 2007/2008)

6.1.3 Overview of the Semiconductor Industry

The semiconductor industry has been constantly evolving since the introduction of the first IC in the early 1970s. Early small-scale integration was mounted with only up to 100 electronic components per chip. Medium-scale integration increased the number of electronic components to 3,000, broadening the range of integrated logic available for computing and logic functions. Subsequently, the advent of large-scale integration had incorporated even larger logic functions (up to 100,000 electronic components), marking the manufacturing of the first microprocessor on a single chip. Eventually, very large-scale integration ("VLSI") that harbours over 100,000 transistors on a chip was made available in the market in the 1980s. Microprocessors with cache memory and floating point arithmetic units signified the contribution of VLSI. Today, to reflect further growth of the complexity, the term ultra large-scale integration was coined for chips with more than 1 million electronic components built-in.

Historically, most if not all, semiconductor companies are vertically integrated across the industry value chain in that they design, fabricate, package and test semiconductors primarily in their own facilities. Advances in technology, competitive pressures as well as the increasingly high labour and capital costs, however, have contributed to a reshaping of the industry which saw the emergence of the specialisation and outsourcing models, as well as the segmentation of the industry along geographical lines.

High labour costs in their developed home countries have prompted many major semiconductor companies to shift the labour-intensive semiconductor assembly and packaging processes to cheaper, developing countries in the Asia Pacific (ex-Japan) region. Outsourcing became a key trend, which saw an increasing number of semiconductor companies outsourcing part or all stages of the semiconductor manufacturing process to independent third parties. Several factors are driving this trend, including the increasing complexity and capital investment required in semiconductor manufacturing as well as competitive and time-to-market pressures. Also, increasing competition has created a need for semiconductor companies to reduce costs and shorten time-to-market, which can be achieved by specialising/focusing their resources on core competencies such as design and marketing, while non-core areas, such as manufacturing, could be outsourced to third parties.

Throughout the years, it is observed that there are advances in manufacturing processes and technologies. These included, among others, the shrinking of IC size of from 0.18µ to 0.13µ, migration from 8-inch to 12-inch wafers and the introduction of new advanced packaging technologies such as flip-chip. As a result, semiconductor manufacturing has become increasingly more complex to the extent that it has become a high technology industry.

The capital investment involved has also ballooned significantly, pushed by the need to continuously upgrade and replace expensive manufacturing equipment with better and more efficient machines to keep up with technological advances and market demands. Since 1984, breakthroughs in EDA technology have improved the productivity of design engineers and rendered computer-automated design possible. Through EDA, chip design has become a more accessible and independent activity. After the introduction of EDA, the decoupling of design from manufacture led to the proliferation of independent fabless design houses. This allows design specialists to no longer worry about the huge amounts of capital.

(Source: IMRR)

6.1.4 IC Design Industry

The IC design industry is a kind of knowledge-intensive manufacturing-supporting service. It creates its innovative competencies and high added value through developing intellectual property. IC design ventures often provide points of entry for talented people who possess new product technologies and intend to start up their own businesses without financial support from the government or big capital. Since the establishment of a small design house needs relatively little capital and few engineers to initiate, most ambitious entrepreneur engineers or technopreneurs venture into this path to enter the semiconductor industry. Some small design houses specialise in certain types of design for customised chips, subcontracting fabrication to the IC manufacturing companies. After the fabrication stage, some design houses do their own testing, while others leave this to the other companies along the semiconductor value chain.

The IC design industry is characterised by specialist companies that are good at a single product. Each IC design company bets on one major product and together they create a diversified and complete design product system. For example, most of the ASIC are used by consumer electronic companies who intend to exploit the advantages of the proprietary IC devices to differentiate their products from those of their competitors.

The rise of ASSPs enriches the variety of IC devices produced in the semiconductor industry. It has allowed IC design houses to design all types of products, from chipsets to LAN sets, for individual customers and for open-market sales. These types of design-intensive and low to medium volume products provide some IC design companies with market niches, in which competitive advantage is based more on timing than on price.

The explosive growth in silicon capacity and consumer usage of electronic products has pressured the design technology communities to quickly harness its potential. The more sophisticated the customer's demands, the more advanced the IC designer's capability must become. Once the customer and chip design house agree on the purpose of a chip, the design process commences. A typical design process includes architecture, logics, circuit, verification, layout, test, approval of design and release to fabrication.

As the costs of low volume semiconductor production decline, application specific design has helped the relatively small design companies to start up and survive. They can be sustained by the large number of medium-sized computer peripheral and consumer product companies who employ both ASICs and ASSPs to help differentiate their products in the market. Thus, IC design houses that accumulate ASIC design capabilities will grasp the opportunities presented by ASICs and be able to take advantage of the trend toward product differentiation in the new competitive arenas.

(Source: IMRR)

6.2 BARRIERS TO ENTRY

6.2.1 High R&D Resource Requirement

Development of SoC requires a massive upfront investment in technology which will discourage potential entrants. Software is one of the major components contributing to the ascending cost. Moreover, there is no real independent software industry to serve this business. The design companies must either develop their own software tools or purchase them from the vendors. After the development of their own software, there is an additional cost element in the registration of IPs or filing of patent for the software.

ASIC designs typically require a substantial investment in NRE costs. NRE cost refers to the one-time cost of engineering effort or product development in ASIC design, a fixed expense associated with a customer-specific adaptation of a standard application / product. Due to the fact that ASIC are "application-specific", every new product involves specific designing requirement with the main bulk of cost being the engineering cost. The cost could range from USD500,000 to USD10,000,000 for one structured ASIC designs and higher for ASIC designs. Since this NRE is "fixed", the product is economically feasible only if economies of scale could be achieved as high volume of production would dilute the "fixed" NRE cost.

Apart from trying to achieve high volume, attempting to get the products to the market quickly is another challenge. Some companies have spent years developing a new product, and then found that it is already obsolete by the time it is released. To shorten the "time-to-market", some companies are forced to pay high prices to purchase third party IP/patents from the vendors. This will increase the production cost inevitably and reduce the profit for the companies.

6.2.2 Shortage of Skilled Personnel

R&D in the IC design houses entails high expertise to operate and lead the team, which is not easy to be built, and costly to maintain. Some big companies commission hundreds of engineers for numerous years to develop the tools needed. Factors like intense competition and technological innovations continuously drive the demand for skilled personnel. In addition, due to rapid technology changes, skilled personnel have to be constantly trained to keep up with the latest developments.

The pool of chip designers available in the Malaysian job market is quite limited. Also, there are very few local universities that offer courses dedicated to aspiring chip designers. The problem with the shortage of skilled personnel is compounded by the fact that fresh university graduates are often given only very fundamental training. They would thus need a few years of hands-on and on-the-job experience to be able to function as capable chip design engineers. Although these engineers are given training by their employers, their retention is another issue. Sometimes, the local fabless companies may have to engage skilled personnel from abroad, incurring higher overheads.

6.2.3 Patents and IPs

The blocks of logic or data that are used in making an ASIC for a product is described as IP cores. The trend of implementing entire systems on an ASIC is creating a market for IP cores. There are designs created by leading third parties, offered access in catalogues, and sold to users for incorporation into large systems. By using these IP cores, a customer can essentially reduce its time-to-market and engineering effort.

A company that has the capability to build its own IP cores forms one of the strongest barriers to entry to new entrants and raises the competitive bar against those who lack the capability. Completed designs with documented IPs not only can be re-used within the company but also marketed to third parties if needed. The advantages of a company having its own IP cores include lower development cost and shorter time-to-market.

Although the current practice of documenting IP cores involves large up-front licensing and processing fees reminiscent of ASIC NRE charges, it has still become increasingly important to control design complexity and to protect the manufacturer's / designer's benefits.

6.2.4 Need for Specialisation

The semiconductor industry is a vast industry with numerous end user application markets such as consumer electronics, IT, automotive, medical devices, etc. Hence the design and technological skills have become more specialised to cater for a specific application market, with application-specific domain knowledge and experiences being compulsory. Designing ASIC for certain specific application markets requires more than generic knowledge. For application markets such as aerospace, medical, automotive, etc., specific knowledge and technological skills acquired by incumbent players form a barrier to entry for companies involved in other markets to venture into the markets dominated by the incumbents. In addition, to differentiate itself from other similar IC design houses, there must be competitive strengths in terms of speed, cost, flexibility and quality of providing design implementation services.

(Source: IMRR)

6.3 GOVERNMENT LEGISLATIONS, POLICIES AND INCENTIVES

6.3.1 Legislations

To encourage the development of a knowledge-based nation, the Government is committed to providing a comprehensive regulatory framework to protect IPs and encourage innovation, facilitating the development of an effective and efficient multimedia environment in Malaysia. IP protection comprises patents, trademarks, industrial designs, copyrights and layout designs of integrated circuits. Components of the Government's regulatory framework include, inter alia:

Patent Act 1983

In accordance with trade-related aspects of intellectual property rights ("TRIPS"), the Patent Act 1983 stipulates that the protection period of a patent is 20 years from the date of filing of an application. Under the Patent Act 1983, the utility innovation certificate provides for an initial duration of 10 years protection from the date of filing of the application. The owner of a patent has the rights in relation to the patent to exploit the patented invention, to assign or transmit the patent, and to conclude a license contract.

Trade Marks Act 1976

The Trade Marks Act 1976 provides protection for registered trademarks and service marks in Malaysia. Once registered, only the registered proprietor or registered user of the trademark may use them and infringement action can be initiated against abusers who use marks without consent. The period of protection is 10 years, renewable for a period of every ten years thereafter. The proprietor of the trademark or service mark has the right to deal or assign as well as to license its use.

Industrial Design Act 1996

The Industrial Designs Act 1996 provide that the rights of an owner in respect of a registered industrial design are personal property and are capable of assignment and transmission by operation of the law. Industrial designs must be new and do not include a method of construction or design that is dictated solely by function. Registered industrial designs are protected for an initial period of five years which may be extended for another two 5-year terms, providing a total protection period of 15 years.

Layout Design of Integrated Circuit Act 2000

The Layout Design of Integrated Circuit Act 2000 provides for the protection of layout designs of integrated circuits based on originality, creator's own invention and the fact that the creation is freely created. The duration of protection is 10 years from the date of its first commercial exploitation or 15 years from the date of creation. The Layout Design of Integrated Circuit Act 2000 is implemented in compliance with the TRIPS agreement to provide a guarantee to investors in Malaysia's electronics industry and to ensure the growth of technology in the country.

Copyright Act 1987

The Copyright Act 1987 is to make better provisions in the law relating to copyright. Literary works, musical works, artistic works films, sound recordings, broadcasts and derivative works is protected automatically if sufficient effort has been expended to make the work original in character and the work has been written down, recorded or otherwise reduced to a material form. The Copyright Act 1987 also specifies the circumstances amounting to and remedies for infringements and offences. The Copyright (Amendment) Act 1997 which amended the Copyright Act 1987, provides for unauthorised transmission of copyright works over the Internet as an infringement of copyright. It is also an infringement of copyright to circumvent any effective technological measures aimed at restricting access to copyright works.

6.3.2 Policies

Under the 9MP, the Government will continue to promote the development of the electronics industry, in view of its extensive linkages to the national economy. Besides attracting the multinational corporations ("MNCs"), the domestic manufacturers will be encouraged to focus on improving the sophistication level of their products, in terms of quality, functionality and design. This is to facilitate the development of the relevant skill sets and expertise, technology know-how and R&D capabilities to move the electronics industry further up the value chain.

As many of these supporting industries to the electronics industry falls under the small-medium enterprise ("SME") category, the government plans to formulate strategies that will propel the SMEs up the value chain into strong knowledge-intensive and value creating entities in the manufacturing sector, so as to meet the challenges of globalisation. There will be increased emphasis placed on technology development capabilities to establish technological leadership, achieve product and services differentiation as well as to create a larger number of local technology-based companies. This is through the provision of appropriate infrastructure, technology transfer and better access to financing. The R&D focus in the semiconductor industry is anticipated to cover fabrication, test and failure analysis, digital and analogue design of IC and advanced microelectronics.

Under the Third Industrial Master Plan 2006-2020 ("IMP3"), the electronics industry is envisaged to continue to grow and contribute significantly to industrial progress and transformation. The MNCs will continue to assume a significant role in increasing the technology level of the industry, in tandem with the global trend in miniaturisation and convergence of technologies in multifunctional product. Testing activities will be part of the development of the entire semiconductor value chain. Towards realising the objectives and targets set for the electronics industry, 7 strategic thrusts have been established and they are as follows:

- Strengthening the semiconductor industry through the establishment of a fully developed semiconductor cluster covering the north-western corridor in the peninsula, including Penang, Perak, Kulim High Technology Park and the neighbouring industrial areas of Kedah;

- Enhancement of the information and communications technology ("ICT") industry value chain. The value chain, presently centred around the MSC in the Klang Valley, will be progressively expanded to designated areas around the country;

- Intensifying specialisation of R&D and design activities and the creation of R&D centres in the public universities and research institutes, so as to facilitate the development of new and emerging technologies;

- Promoting the application of new and emerging technologies like nanotechnology, micro electromechanical systems, photonics, wireless technologies and advanced display technologies to encourage the improvement of the competitiveness of domestic companies;

- Measures will be undertaken to nurture the existing domestic companies with the growth potential to expand and integrate into the regional and global supply chain networks, as well as become major producers on their own;

- Making available a sufficient supply of highly skilled and innovative workforce

- Strengthening the institutional support for the development of the electronics industry which includes the formulation of a standardised quality control management system, management and disposal of scheduled wastes and strengthening the role of industry associations.

6.3.3 Incentives

I Incentives for MSC status companies

MSC status is the recognition by the Government through the MDeC to companies that participate and undertake ICT activities in the MSC. Companies with MSC status enjoy a set of incentive and benefits that is backed by the Government's Bill of Guarantees.

The incentives enjoyed by MSC status companies are:

- Pioneer status with a tax exemption of 100% of the statutory income for a period of five years for the first round, or an Investment Tax Allowance ("ITA") of 100%, and

- Eligibility of R&D grants (for majority Malaysian-owned MSC status companies).

Other benefits include:

- Duty free import of multimedia equipment;
- IP protection and a comprehensive framework of cyberlaws;
- No censorship of the Internet;
- Globally competitive telecommunication tariffs and services;
- High-powered implementation agency, the MDeC, to provide consultancy and assistance within the MSC;
- High quality, planned urban development;
- Excellent R&D facilities; and
- Green and protected environment.

Key ASIC obtained its MSC status from MDeC on 14 April 2006 and currently is enjoying full income tax exemption under the pioneer status for a period of 5 years and is renewable for another 5 years term.

II Incentives for a Knowledge-based Economy

Malaysia is in the process of transforming itself from a production-based to a knowledge-based economy. To further encourage companies to invest in knowledge-intensive activities, certain companies that qualify will be granted "Strategic Knowledge-based Status". These companies must have the following characteristics:

- The potential to generate knowledge content;
- High value-added operations;
- Usage of high technology;
- A large number of knowledge-based workers; and
- Possess a corporation knowledge-based master plan.

Companies granted "Strategic K-based Status" are eligible for the following incentives:

- Pioneer status with a tax exemption of 100% of the statutory income for a period of 5 years; or
- ITA of 60% on the qualifying capital expenditure incurred within 5 years. The allowance can be offset against 100% of the statutory income in the year of assessment.

III Incentives for R&D

To further strength Malaysia's foundation for more integrated R&D, companies which carry out design and prototyping as independent activities are also eligible for incentives.

Main Incentives for R&D

a. Contract R&D Company

A contract R&D company, i.e., a company that provides R&D services in Malaysia to a company other than its related company, is eligible for:

- Pioneer status with a tax exemption of 100% of the statutory income for 5 years; or
- ITA of 100% on the qualifying capital expenditure incurred within 10 years, which can be offset against 70% of the statutory income in the year of assessment.

b. R&D Company

A R&D company, i.e. a company that provides R&D services in Malaysia to its related company or to any other company, is eligible for an ITA of 100% on the qualifying capital expenditure incurred within 10 years. The allowance can be offset against 70% of the statutory income in the year of assessment. Should the R&D company opt not to avail itself of the allowance, its related companies can enjoy a double deduction for payments made to the R&D company for services rendered.

Eligibility:

- Research undertaken should be in accordance with the needs of the country and bring benefit to the economy;
- At least 70% of the income of the company should be derived from R&D activities;
- For manufacturing-based R&D, at least 50% of the workforce of the company must be appropriately qualified personnel performing research and technical functions; and
- For agriculture-based R&D, at least 5% of the workforce of the company must be appropriately qualified personnel performing research and technical functions.

c. In-House Research

A company that undertakes in-house R&D to further its business can apply for an ITA of 50% on the qualifying capital expenditure incurred within 10 years. The company can offset the allowance against 70% of its statutory income in the year of assessment.

d. Second Round Incentives

R&D companies/activities mentioned in categories (i) - (iii) will be eligible for a second round of Pioneer status for another five years, or ITA for a further 10 years, where applicable.

6. INDUSTRY OVERVIEW *(CONT'D)*

e. Double Deduction for R&D

- A company can enjoy a double deduction on its revenue (non-capital) expenditure for research which is directly undertaken and approved by the Minister of Finance;
- Double deduction can also be claimed for cash contributions or donations to approved research institutes, and payments for the use of the services of approved research institutes, approved research companies, R&D companies or contract R&D companies;
- Approved R&D expenditure incurred during the Pioneer Status period will be allowed to be accumulated and brought forward and be given another deduction after the Pioneer Status period; and
- Expenditure on R&D activities undertaken overseas, including the training of Malaysian staff, will be considered for double deduction on a case-by-case basis.

(Source : IMRR)

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6.4 MAJOR PLAYERS AND COMPETITION

There are a total of 15 local fabless IC design houses in Malaysia, mostly located and operating in the MSC area. This number excludes the MNCs located in Malaysia such as Intel that possess fabless houses that design ICs primarily to meet their own internal requirements.

The total revenue generated by the major local fabless IC design houses amounted to approximately RM130 million in 2006. These fabless companies in Malaysia are relatively new and small (some with less than 10 employees). Although most of them employ both analogue and digital technology (thus theoretically enabling them to produce all analogue, mixed signals and digital products), their product range is more focused, with each of them trying to establish themselves in their respective niche application markets. Our Group ranked first among the local fabless IC design houses, with an estimated market share of 39.1% in 2006.

On the international front, the fabless market is a huge market with revenue registering approximately USD50 billion in 2006, up 27% from USD39 billion registered in 2005. Some of the major international fabless IC companies with business activities that are comparable to our Group are Faraday Technology Corporation, LSI Corporation, Mediatek Inc., Vimicro International Corporation and ALi Corporation. Their business activities primarily focus on the research, design, development and marketing of complex high-performance ICs including, but not limited to, SoC, analogue, digital and mixed-signal ASIC/ASSP products. Their IPs and ICs target the consumer electronics, multimedia and communication application markets. Collectively, these companies registered around USD6.1 billion in revenue and USD1.2 billion in PAT as at their latest respective financial reporting dates.

(Source: IMRR)

6.5 SUBSTITUTE PRODUCTS

There is no direct substitute for the analogue, digital and mixed signal ASIC due to the versatility and the increasing complexity of the designs as the IC industry continues to grow. Unlike the market for digital ASICs which is characterised by a very large number of suppliers and by the readiness of customers to switch suppliers if they are offered a better combination price/performance ratio, analogue/mixed signal ASIC solution providers and their customers strive to build mutually beneficial partnerships.

SoC devices are primarily dedicated devices designed to penetrate a mature, high-volume market, where the potential life expectancy of a product is relatively long and there is no need to continuously improve the SoC. This is due to its relatively longer time-to-market and higher development cost as compared to its closest substitute, the System-in-Package ("SiP"). However, the primary advantages of selecting SoC technology are due to its high performance, higher levels of device integration and high volume vis-à-vis SiP.

(Source: IMRR)

6.6 PROSPECTS AND OUTLOOK OF THE INDUSTRY

6.6.1 Key Industry Growth Drivers

The fabless semiconductor industry has been the segment with the highest growth rate for the past few years in the semiconductor industry. For the 5-year period from 2002 to 2006, this particular segment of the industry achieved an impressive 36% compound annual growth rate in revenue. For 2006, the fabless revenue was reported to be approximately USD50 billion which translated to a 27% year-on-year growth. Worldwide SoC market is estimated to be worth more than USD43 billion by 2009.

6.6.2 Expanding Semiconductor Market

The constant growth of the global economy has ensured the expansion of the semiconductor market. Global sales of semiconductors increased by 8.9% in 2006, mainly due to strong growth in consumer electronics and favourable economic conditions in the major world markets.

China is a critical component of the global semiconductor industry, and is expected to increase its worldwide semiconductor market share to 26% in 2008 driven by the growth of wafer manufacturing plants and fabless companies. The country has become the manufacturing base for the global consumer electronics industry.

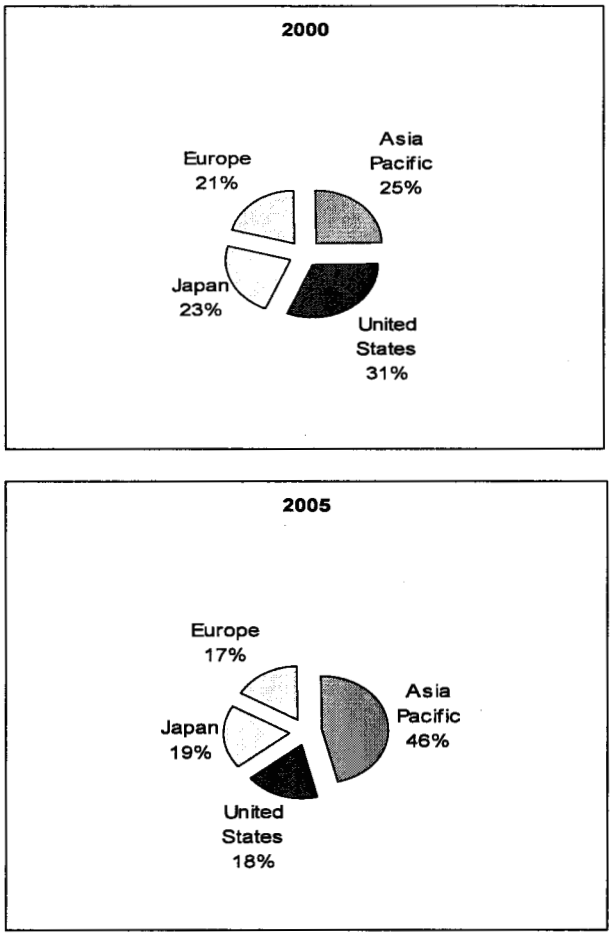
The high energy prices that have dampened the economy growth in 2005 and 2006 did not affect consumer demand for electronics as bad as was originally anticipated. Conversely, the demand for the end products became much stronger than expected. Wireless handset sales hit 23% growth in 2006 with similar strong increases in the sales of digital televisions, digital cameras and MP3 players.

After 2 quarters of sluggish sales, the electronics industry in Malaysia is experiencing an increase in orders for its products in the second half of 2007. Going forward, amid a sudden surge in demand, there could be a shortfall of foundry capacity worldwide by the end of 2007 and into 2008.

6.6.3 Strong Growth in the Asia Pacific Market

The Asia Pacific has been an increasingly important market for the semiconductor industry with an increasing worldwide market share. This market possesses tremendous opportunities for companies operating in the semiconductor industry, especially with the increasing outsourcing activities in the region. The Asia Pacific region's (ex-Japan) market share to total worldwide semiconductor sales has grown from 25% in 2000 to 46% in 2005.

Semiconductor Sales by Region



Source: D&B Malaysia Research

6.6.4 Increasing Capital Investments

Compared to the general semiconductor industry's market which is highly cyclical in nature, the fabless segment has been enjoying high growth for the past few years. This trend is expected to continue and gain further momentum. As a result, fabless companies are attracting investors to provide capital investments with the expectation of good returns. The availability of funds will be a catalyst to R&D activities and is beneficial to the market growth.

6.6.5 Technological Advances

The other important growth factor of the semiconductor industry is technological advances. The semiconductor industry allocates significant amount of funds for R&D. The advances in basic knowledge then fuel the industrial progress. It is remarkable that, despite significant technological challenges, the industry is able to maintain the pace predicted by Moore's Law - the doubling of transistors every 2 years. At the same time, transistor speed continued to improve at the record improvement rate of 17% per year. The rapid technological advancements enable the industry to widen the application markets, lower the price of the end products and introduce new products. The advent of innovative products has also created new markets.

6.6.6 New Emerging Market Segments

New emerging market segments include the medical and aerospace industries. Due to the ageing global population, the demand for healthcare products in both developed and developing countries has steadily increased. Advances in technology are giving rise to new therapeutic modalities, which in turn are addressing more medical problems and aiding in prevention, early diagnosis and intervention of diseases. As a result, hefty investments have been injected into the semiconductor industry for the development of implantable medical devices, hearing aids, medical imaging systems, patient monitoring systems, and other applications.

The overall aerospace and military industry is experiencing positive growth especially after the 911 tragedy. Predictably, this segment of the industry suffers from IC component obsolescence and is requiring constant system reviews and updates.

(Source: IMRR)

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7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL

7.1 DIRECTORS

7.1.1. Profiles

The profiles of our Directors are as follows:

Eg Kah Yee, a Malaysian, aged 47, was appointed to our Board as a Non-Independent Non-Executive Chairman on 15 June 2006. He graduated with Bachelor of Computer Science degree from West Virginia University, USA in 1983. He started his career as a R&D Engineer with Phoenix Data Systems Inc., Santa Clara, California, USA, before joining Daisy Systems Corporation ("Daisy"), a company listed on the NASDAQ Market and a pioneer in computer aided engineering in electronic designs, as R&D Project Manager.

While he was in Daisy, he assumed various positions as Regional Technical Director, Country Manager (Taiwan) and Director of North Asia Region. In 1990, he joined Synopsys Inc., a company listed on the NASDAQ Market, which pioneered the high level design for ASIC and VLSI, as Regional Manager for South Asia Pacific Operations and was subsequently promoted as General Manager for Asia Pacific Operations in 1992. He left Synopsys Inc. in 1996 and founded Palette Multimedia Berhad in 1997 and has been the Chairman/Managing Director since then. Currently, he is the Chairman of Malaysia IC Design Association and he also sits on the board of directors of Anchor Bay Technology Inc, Jaalaa Inc, Silterra, AQSB and various private limited companies.

Jalaluddin bin Mohd Jarjis, a Malaysian, aged 52, was appointed to our Board as a Non-Independent Non-Executive Director on 7 August 2006. He graduated with a Bachelor of Physics and Mathematics degree from Drew University, New Jersey, USA in 1977. He spent over 15 years in research work in theoretical physics and mathematics in USA, Europe, New Zealand and United Kingdom before joining Jardine Fleming, a British Hong Kong Investment Bank in 1999 as an Investment Analyst and left the bank in the same year. In 2001, he formed Artisan Encipta Ltd, a venture capital company in which he serves as Principal and Chairman. In July 2004, he was appointed by Khazanah as Chairman of Silterra. He currently also serves as a Technology Advisor to Khazanah. In December 2005, he was made the Chairman of AQSB, a wholly-owned subsidiary of Khazanah, and heads the Investment Executive Team in AQSB.

Benny T. Hu (also known as Ting Wu Hu), a Taiwanese, aged 58, was appointed to our Board as a Non-Executive Director on 4 November 2006 and subsequently re-designated as our Independent Non-Executive Director on 4 October 2007. He graduated with a Master in Business Administration degree from Wharton School, University of Pennsylvania in 1978. He started his career as a Manager in Bankers Trust Company. He has more than 25 years of experience in finance and investment industry. He was the President and later Chairman of China Development Industrial Bank, the largest venture capital firm in Taiwan with an investment portfolio over USD3 billion, from 1993 to 2004. The investment portfolio consists of over 500 investee companies, in which 80% of them are IT-related companies. He has been actively involved in the semiconductor industry and was a former Vice Chairman and founder of World Semiconductor Manufacturing Corporation from 1996 to 2001. He has been a member of Rand Corporation Asia Pacific board and a board member of Stanford Institute for Economic Policy Research since 2000. Currently, he is the Chairman of National Taiwan University Incubation Centre, which the main objective is to provide financial and operational assistance to Taiwan's ever-growing IT- related companies.

In addition, he also chairs multiple IC or semiconductor related companies or focused venture funds.

Henry Choo Hon Fai, a Malaysian, aged 35, was appointed to our Board as a Non-Independent Non-Executive Director on 4 November 2006. He graduated with a Bachelor of Science degree in Computer Science from La Trobe University, Melbourne, Australia in 1993. He started his career as an Equity Research Analyst in Dao Heng Securities Ltd, Hong Kong in 1994. He has more than 9 years of direct investment and operations experience within the venture capital and securities industry in Hong Kong and Malaysia. He was appointed as Director in Fok Lee Sdn Bhd from 1996 to 2000 and a senior analyst in Intelligent Capital Sdn Bhd from 2000 prior to joining Artisan Encipta Ltd in 2003. He also spent 3 years working in senior management and business development roles in the building industry from 1996 to 1999. Currently, he is an Independent Non-Executive Director at Mudajaya Group Berhad and Mulpha Land Berhad. He is also the Chief Operating Officer and Vice-President for Investments of AQSB. He also serves as the Executive Assistant to the Chairman of Silterra.

Lai Yit Loong, a Malaysian, aged 43, was appointed to our Board as a Non-Executive Director on 2 November 2006 and subsequently re-designated as our Independent Non-Executive Director on 4 October 2007. He graduated with a Bachelor of Science degree from the National University of Singapore in 1987. He started his career as a network and systems integration consultant with Hewlett-Packard, Singapore in 1988. He was employed by Computer Associates Malaysia as their Country Sales Manager in 1994. Subsequently, he joined Intel Malaysia and started the sales and marketing office in 1996. Since then, he had assumed various senior positions at Intel Malaysia. He was a Technical Assistant to Intel Asia Pacific's Vice President and General Manager from 1998 to 1999. After that, he worked at the company's head office in Santa Clara, California as worldwide e-Business Program Manager from 1999 to 2000. His last job was as a Country Manager for Intel China from 2004 to 2006, where he was responsible for the expansion of Intel capabilities and businesses. He was awarded the Intel Achievers Award in 2005 for his innovation in driving computer adoption in emerging markets. In 2006, he joined Nvidia as their Vice-President of Taiwan and South Asia Sales, where he was responsible for graphics and core logic design, sales and business development in Taiwan, South East Asia, Australia and New Zealand. He joined Silterra in 2007 as their Vice-President of worldwide sales and marketing. He is currently based in Taiwan.

See Chin Lam, a Malaysian, aged 38, was appointed to our Board as a Non-Independent Non-Executive Director on 7 August 2006 and subsequently re-designated as our Independent Non-Executive Director on 26 November 2007. He graduated with a Bachelor of Engineering degree in Mechanical and Manufacturing Engineering from the University of Melbourne, Australia. He started his career in the Semiconductor Products Sector of Motorola Malaysia Sdn Bhd in 1992 and he last held the position of a Senior Engineer after 5 years of service. He then joined CAVSB in 1997 and had been involved in sourcing, evaluating, structuring, investing, managing and exiting investments in the information and communication technology, advanced manufacturing, life sciences and services sectors for over 10 years, primarily managing the CTVSB portfolio and serving as non-executive director on various investee companies of CTVSB. He last held the position of Executive Director at CAV Private Equity Management Sdn Bhd (a subsidiary of

CAVSB) until 23 November 2007. He is currently a Partner in Vida Partners Sdn Bhd.

N. Chanthiran a/l Nagappan, a Malaysian, aged 43, was appointed to our Board as an Independent Non-Executive Director on 14 December 2007. He graduated with a Bachelor of Accounting (Honours) degree from University of Malaya in 1988. He is also a Chartered Accountant, Certified Public Accountants, Certified Risk Professional and Certified Financial Planner. He started his career as tax executive in Coopers & Lybrand in 1988. In 1994, he joined Arab Merchant Bank Berhad as Assistant Manager. In 1995, he worked as Corporate Finance Manager with Sadec Group. He started his Audit practice in 2001. He has more than 17 years of corporate finance experience in the areas of listing, financial and corporate restructuring, mergers and acquisition. Currently, he is a partner of Chanthiran & Co. and CH & Associates. He is also an Executive Director of Lityan Holdings Berhad.

7.1.2 Shareholdings in our Company

The direct and indirect shareholdings of our Directors before and after the Public Issue are as follows:

	<---------- Before the Public Issue -------->				<---------- After the Public Issue ---------->			
	<---- Direct ----->		<------- Indirect -------->		<----- Direct ------->		<------- Indirect -------->	
	No. of Shares	%	No. of Shares	%	No. of Shares	%	No. of Shares	%
Eg Kah Yee	-	-	(1)413,000,000	68.49	-	-	(1)413,000,000	51.31
Jalaluddin bin Mohd Jarjis	-	-	-	-	-	-	-	-
Benny T. Hu	-	-	-	-	-	-	-	-
Henry Choo Hon Fai	-	-	-	-	-	-	-	-
Lai Yit Loong	-	-	-	-	(2)50,000	0.01	-	-
See Chin Lam	-	-	-	-	-	-	-	-
N. Chanthiran a/l Nagappan	-	-	-	-	-	-	-	-

Notes:

(1) *Deemed interested by virtue of his interest in KAGL, the holding company of KAL, pursuant to Section 6A of the Act.*

(2) *Represents the number of Key ASIC Shares allocated pursuant to the pink form portion under the Retail Offering and assuming that the eligible Director will subscribe to the Key ASIC Shares in full.*

7.1.3 Previous or Existing Directorships and Substantial Shareholdings in other Public Companies

Save as disclosed below, none of our Directors hold any directorship or is a substantial shareholder in any public companies for the past 2 years preceding the date of this Prospectus:

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

		<----------Directorship---------->			Substantial shareholdings as at <---------- 30 November 2007 ----------> <--------Direct---------->		<--------Indirect-------->	
Name	**Company**	**Position**	**Date of appointment**	**Date of resignation / retirement**	**No of ordinary shares held**	**%**	**No of ordinary shares held**	**%**
Eg Kah Yee	Palette Multimedia Berhad	Chairman/ Managing Director	07.05.1998	-	29,133,621	4.83	(1) 767,179	0.13
Henry Choo Hon Fai	Mudajaya Group Berhad	Director	02.03.2004	-	-	-	-	-
	Mulpha Land Berhad	Director	13.09.2007	-	-	-	-	-
Jalaluddin bin Mohd Jarjis	IC Microsystems Corp Berhad	Director	18.04.2005	-	-	-	-	-
N. Chanthiran a/l Nagappan	Lityan Holdings Berhad	Director	24.10.2007	-	-	-	-	-

Note:

(1) Deemed interested by virtue of his interest in Digital Season Sdn Bhd and his brother, Eg Kaa Chee's shareholdings in Palette Multimedia Berhad.

7.1.4 Directors' Remuneration and Benefits

There was no remuneration and benefits-in-kind paid to our Directors for the FYE 2006. We estimate and forecast to pay approximately RM0.10 million and RM0.14 million in remuneration and benefits-in-kind to our Directors for the FYE 2007 and the FYE 2008 for services rendered to our Group in all capacities as follows:

Directors	<---------- FYE ---------->		
	<-------- 2006 ------>	<-------- 2007 ------>	<-------- 2008 ------>
Eg Kah Yee	-	Band 1	Band 2
Jalaluddin bin Mohd Jarjis	-	*Band 1	*Band 1
Benny T. Hu	-	Band 1	Band 1
Henry Choo Hon Fai	-	*Band 1	*Band 1
Lai Yit Loong	-	Band 1	Band 1
See Chin Lam	-	*Band 1	Band 1
N. Chanthiran a/l Nagappan	-	Band 1	Band 1

Notes:

* *Paid directly to the investment holding company*

Band 1 : Up to RM50,000 per annum

Band 2 : Between RM50,001 and RM100,000 per annum

Our Directors' remuneration is approved by our Board and the shareholders of our Company following recommendations made by our Remuneration and Nomination Committee.

7.1.5 Board Practice

Our Directors are appointed by our shareholders at a general meeting and election of Director takes place annually. Under our Articles of Association, one-third (1/3) of our Directors are subject to retirement by rotation at each annual general meeting but are eligible for re-appointment. Further, all our Directors are required to retire from office at least once in every 3 years. Any person appointed as a Director, either to fill a casual vacancy or as an addition to the existing Directors, shall hold office until the next annual general meeting, and shall then be eligible for re-election.

In accordance with Article 84 of our Articles of Association, our Directors shall retire from office and offer themselves for re-election at the next annual general meeting in accordance with the above foregoing provisions provided there is no change in the directorships from the date of issue of this Prospectus to the next annual general meeting.

7.1.6 Audit, Remuneration and Nomination Committees

(a) Audit Committee

The members of our Audit Committee are as follows:

Name	Designation	Directorship
Benny T.Hu	Chairman	Independent Non-Executive Director
Lai Yit Loong	Member	Independent Non-Executive Director
N. Chanthiran a/l Nagappan	Member	Independent Non-Executive Director

The main functions of our Audit Committee include the following:

(i) review the audit plans, audit reports, auditors' evaluation of our internal accounting controls and our financial statements;

(ii) monitor the independence and qualification of our Company's independent auditors;

(iii) review any related party transactions entered into by our Group and any conflict of interest situations that may arise within our Group; and

(iv) monitor our compliance with relevant laws, regulations and code of conduct.

(b) Remuneration and Nomination Committee

The members of our Remuneration Committee are as follows:

Name	Designation	Directorship
Eg Kah Yee	Chairman	Non-Independent Non-Executive Director
Henry Choo Hon Fai	Member	Non-Independent Non-Executive Director

The members of our Nomination Committee are as follows:

Name	Designation	Directorship
Jalaluddin bin Mohd Jarjis	Chairman	Non-Independent Non-Executive Director
See Chin Lam	Member	Independent Non-Executive Director

The main functions of our Remuneration and Nomination Committee are as follows:

(i) recommend candidates for appointment to our Board and key management positions;

(ii) provide assistance and guidance to our Board in determining and recommending the remuneration package of each Director and certain key management personnel, compensation strategy and management development;

(iii) establish the performance criteria to evaluate the performance of our Directors; and

(iv) ensure corporate accountability and governance in respect of our remuneration and compensation functions.

7.1.7 Our Executive Directors' Involvement in Other Businesses/Corporations

None of the members of our Board is a Director who is currently involved in a full time executive position in our Group.

7.2 PROMOTERS AND SUBSTANTIAL SHAREHOLDERS

7.2.1 Profiles

Our Promoters and substantial shareholders are KAL, AQSB and CTVSB. The profiles of our Promoters and substantial shareholders are as follows:

KAL was incorporated in British Virgin Islands on 2 September 2005 as a private limited company. The principal activity of the company is investment holdings and sales and marketing of IP and IC products.

As at 30 November 2007, the authorised share capital of KAL is USD20,000,000 comprising 200,000,000 ordinary shares of USD0.10 each, whereas the issued and paid-up share capital is USD15,200,000 comprising 152,000,000 ordinary shares of USD0.10 each in KAL.

The details of the director and substantial shareholders of KAL and their respective shareholdings are as follows:

		<---------- Direct ---------->		<----------Indirect---------->	
	Nationality/ Place of incorporation	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**
Director					
Eg Kah Yee	Malaysian	-	-	(1)70,000,000	46.0
Substantial shareholders					
KAGL	Malaysian	70,000,000	46.0	-	-
PSL	Taiwan	26,000,000	17.1	-	-
TCPL	Canada	26,000,000	17.1	-	-
Eg Kah Yee	Malaysian	-	-	(1)70,000,000	46.0
Chang Tao-Chun	Taiwanese	-	-	(2)26,000,000	17.1
Fang Chun-Jung	Canadian	-	-	(3)26,000,000	17.1
Chang Li-Ping	Canadian	-	-	(3)26,000,000	17.1

Notes:

(1) *Deemed interested by virtue of his interest in KAGL, the holding company of KAL, pursuant to Section 6A of the Act.*

(2) *Deemed interested by virtue of his interest in PSL pursuant to Section 6A of the Act.*

(3) *Deemed interested by virtue of their interest in TCPL pursuant to Section 6A of the Act.*

Eg Kah Yee is a Director and substantial shareholder of KAL. His experience in the IC design industry is set forth in Section 7.1.1 of this Prospectus.

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

AQSB was incorporated in Malaysia on 7 November 2005 under the Act as a private limited company and is a wholly-owned subsidiary of Khazanah, the investment arm of the Malaysian Government. The principal activity of the company is investment holding.

As at 30 November 2007, the authorised share capital of AQSB is RM400,000,000 comprising 400,000,000 ordinary shares of RM1.00 each, whereas the issued and paid-up share capital is RM152,271,900 comprising 152,271,900 ordinary shares of RM1.00 each in AQSB.

The details of the directors and substantial shareholder of AQSB and their respective shareholdings are as follows:

		<---------- Direct --------->		<-------- Indirect ---------->	
	Nationality/ Place of incorporation	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**
Directors					
Jalaluddin bin Mohd Jarjis	Malaysian	-	-	-	-
Eg Kah Yee	Malaysian	-	-	-	-
Yeo Keng Un	Malaysian	-	-	-	-
Substantial shareholder					
Khazanah	Malaysia	152,271,900	100.00	-	-

CTVSB was incorporated in Malaysia on 25 April 2000 under the Act as a private limited company. The principal activity of the company is the provision of equity and mezzanine capital to viable, innovative, high growth and emerging companies. CTVSB is jointly funded by Bank Negara Malaysia and CIMB Bank Berhad ("CIMB Bank") to spur technology financing and promote its development in Malaysia.

As at 30 November 2007, the authorised share capital of CTVSB is RM1,000,000 comprising 250,000 ordinary shares of RM1.00 each and 750,000 preference shares of RM1.00 each, whereas the issued and paid-up share capital is RM152,000 comprising 2,000 ordinary shares of RM1.00 each and 150,000 preference shares of RM1.00 each in CTVSB.

CIMB Bank holds all the issued preference shares in CTVSB and CAVSB holds all the ordinary shares in CTVSB.

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

The details of the directors and substantial shareholder of CTVSB are as follows:

	Nationality/ Place of incorporation	<---------- Direct --------> No. of ordinary shares	%	<-------- Indirect ----------> No. of ordinary shares	%
Directors					
Jamil Hajar bin Abdul Muttalib	Malaysian	-	-	-	-
Vijayaledchumy a/p T.Veluppillai	Malaysian	-	-	-	-
Daniel Hoh Yuen Leong	Malaysian	-	-	-	-
Darawati Hussain	Malaysian	-	-	-	-
Ng Ing Peng	Malaysian	-	-	-	-
Raja Noorma binti Raja Othman (Alternate Director to Ng Ing Peng)	Malaysian	-	-	-	-
Substantial shareholder					
CAVSB	Malaysia	2,000	100.00	-	-

KAGL was incorporated in British Virgin Islands on 29 August 2005 as a private limited company and is wholly-owned by Eg Kah Yee. The principal activity of the company is investment holding.

As at 30 November 2007, the authorised share capital of KAGL is USD50,000 comprising 50,000 ordinary shares of USD1.00 each, whereas the issued and paid-up share capital is USD1.00 comprising 1 ordinary shares of USD1.00 each in KAGL.

The details of the director and substantial shareholder of KAGL and their respective shareholdings are as follows:

	Nationality/ Place of incorporation	<---------- Direct ---------> No. of ordinary shares	%	<-------- Indirect ----------> No. of ordinary shares	%
Director					
Eg Kah Yee	Malaysia	1	100.00	-	-
Substantial shareholder					
Eg Kah Yee	Malaysia	1	100.00	-	-

PSL was incorporated in British Virgin Islands on 23 November 1999 as a private limited company and is wholly-owned by Chang Tao-Chun. The principal activity of the company is investment holding.

As at 30 November 2007, the authorised share capital of PSL is USD50,000 comprising 50,000 ordinary shares of USD1.00 each, whereas the issued and paid-up share capital is USD50,000 comprising 50,000 ordinary shares of USD1.00 each in PSL.

The details of the director and substantial shareholder of PSL and their respective shareholdings are as follows:

		<---------- Direct --------->		<-------- Indirect ---------->	
	Nationality/ Place of incorporation	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**
Director					
Wang Hsu-Ying	Taiwanese	-	-	-	-
Substantial shareholder					
Chang Tao-Chun	Taiwanese	50,000	100.00	-	-

TCPL was incorporated in British Virgin Islands on 15 August 2005 as a private limited company. The principal activity of the company is investment holding.

As at 30 November 2007, the authorised share capital of TCPL is USD100,000 comprising 100,000 ordinary shares of USD1.00 each, whereas the issued and paid-up share capital is USD50,000 comprising 50,000 ordinary shares of USD1.00 each in TCPL.

The details of the directors and substantial shareholders of TCPL and their respective shareholdings are as follows:

		<---------- Direct --------->		<-------- Indirect ---------->	
	Nationality/ Place of incorporation	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**
Directors					
Fang Chun-Jung	Canadian/ Taiwanese	25,000	50.00	-	-
Chang Li-Ping	Canadian/ Taiwanese	25,000	50.00	-	-
Substantial shareholders					
Fang Chun-Jung	Canadian/ Taiwanese	25,000	50.00	-	-
Chang Li-Ping	Canadian/ Taiwanese	25,000	50.00	-	-

Eg Kah Yee is a substantial shareholder and Non-Independent Non-Executive Director of our Group. His profile is set forth in Section 7.1.1 of this Prospectus.

Chang Tao-Chun, a Taiwanese, aged 77, obtained his Bachelor of Arts degree from National Taiwan University in 1963. He established PSL in 1999.

Fang Chun-Jung, a Canadian/Taiwanese, aged 51, obtained his Bachelor of Sociology degree from National Taiwan University in 1978. Currently, he is a director in TCPL.

Chang Li-Ping, a Canadian/Taiwanese, aged 43, finished high school in 1982. Currently, he is a director in TCPL.

CAVSB was incorporated in Malaysia on 16 January 1995 under the Act as a private limited company and is a wholly-owned subsidiary of CIMB Group Sdn Bhd ("CIMBG"). The principal activity of CAVSB is provision of equity and mezzanine capital to viable, innovative, high growth and emerging companies.

CIMBG was incorporated on 18 August 2005 under the Act. Its principal activity is investment holding. CIMBG is wholly-owned by Bumiputra-Commerce Holdings Berhad ("BCHB") and is Malaysia's second largest financial services provider through BCHB.

BCHB was incorporated on 24 December 1956 under the Act. The principal activities of BCHB are those of investment holding, management company, property management, provision of consultancy services and dealing in securities. BCHB was listed on the Main Board of Bursa Securities on 3 November 1987.

Khazanah was incorporated on 3 September 1993 as a public limited company under the Act. Khazanah is the investment holding arm of the Government entrusted to manage the assets held by the Government and to undertake strategic investments.

7.2.2 Promoters' and Substantial Shareholders' Shareholdings in our Company

The interests of our Promoters and substantial shareholders in our Shares, before and after the Public Issue are as follows:

	<---------- Before the Public Issue---------->				<---------- After the Public Issue ---------->			
	<------ Direct -------->		<----- Indirect -------->		<--------- Direct ------>		<------ Indirect ------->	
	No. of Shares	%	No. of Shares	%	No. of Shares	%	No. of Shares	%
KAL	413,000,000	68.49	-	-	413,000,000	51.31	-	-
AQSB	133,000,000	22.06	-	-	133,000,000	16.52	-	-
CTVSB	57,000,000	9.45	-	-	57,000,000	7.08	-	-
KAGL	-	-	(1)413,000,000	68.49	-	-	(1)413,000,000	51.31
PSL	-	-	(1)413,000,000	68.49	-	-	(1)413,000,000	51.31
TCPL	-	-	(1)413,000,000	68.49	-	-	(1)413,000,000	51.31
Eg Kah Yee	-	-	(2)413,000,000	68.49	-	-	(2)413,000,000	51.31
Chang Tao-Chun	-	-	(3)413,000,000	68.49	-	-	(3)413,000,000	51.31
Fang Chun-Jung	-	-	(4)413,000,000	68.49	-	-	(4)413,000,000	51.31
Chang Li-Ping	-	-	(4)413,000,000	68.49	-	-	(4)413,000,000	51.31

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

	<---------- Before the Public Issue---------->				<---------- After the Public Issue ---------->			
	<------ Direct -------->		<------ Indirect ------->		<----- Direct -------->		<----- Indirect -------->	
	No. of Shares	%	No. of Shares	%	No. of Shares	%	No. of Shares	%
CAVSB	-	-	[5]57,000,000	9.45	-	-	[5]57,000,000	7.08
CIMBG	-	-	[6]57,000,000	9.45	-	-	[6]57,000,000	7.08
BCHB	-	-	[7]57,000,000	9.45	-	-	[7]57,000,000	7.08
Khazanah	-	-	[8]190,000,000	31.51	-	-	[8]190,000,000	23.60

Notes:

(1) *Deemed interested by virtue of their interest in KAL pursuant to Section 6A of the Act.*

(2) *Deemed interested by virtue of his interest in KAGL pursuant to Section 6A of the Act.*

(3) *Deemed interested by virtue of his interest in PSL pursuant to Section 6A of the Act.*

(4) *Deemed interested by virtue of their interest in TCPL pursuant to Section 6A of the Act.*

(5) *Deemed interested by virtue of its interest in CTVSB pursuant to Section 6A of the Act.*

(6) *Deemed interested by virtue of its interest in CAVSB pursuant to Section 6A of the Act.*

(7) *Deemed interested by virtue of its interest in CIMBG pursuant to Section 6A of the Act.*

(8) *Deemed interested by virtue of its interest in AQSB and BCHB pursuant to Section 6A of the Act.*

7.2.3 Previous or Existing Directorships or substantial shareholdings in other Public Companies

Save as disclosed below, none of our Promoters and substantial shareholders hold any directorship or is a substantial shareholder in any public companies for the past 2 years preceding the date of this Prospectus:

		<----------Directorship---------->			Substantial shareholdings as at <---------- 30 November 2007 ----------> <----------Direct-------->		<------Indirect---------->	
Name	Company	Position	Date of appointment	Date of resignation / retirement	No of ordinary shares held	%	No of ordinary shares held	%
CTVSB	Opensys (M) Berhad	-	-	-	21,544,010	9.65	-	-
	Tricubes Berhad	-	-	-	20,713,906	15.46	-	-
	Carotech Berhad	-	-	-	22,406,976	4.93	-	-
	Wimems Corporation Berhad	-	-	-	21,630,010	8.17	-	-
	NTI International Limited	-	-	-	-	-	[1]12,887,000	8.06

Please refer to Section 7.1.3 of this Prospectus for Eg Kah Yee's previous or existing directorships and substantial shareholdings in other Public Companies

Note:

(1) *CTVSB is deemed to be interested in the 12,887,000 shares held in the name of UOB Kay Hian Pte Ltd.*

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

7.2.4 Changes in the Shareholdings of Our Promoters and Substantial Shareholders

The changes in the shareholdings of our Promoters and substantial shareholders for the past 3 years preceding the date of this Prospectus are as follows:

	<---------- As at 22 August 2005 ---------->				<---------- As at 30 November 2006 ---------->				<---------- As at 30 November 2007 ---------->			
	<--------Direct--------->		<--------Indirect--------->		<---------Direct--------->		<--------Indirect--------->		<---------Direct---------		<-------Indirect------->	
Name	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**	**No. of ordinary shares**	**%**
Tan Wang Tiang	1	50.00	-	-	-	-	-	-	-	-	-	-
Ng Lui Keng @ Ng Joo Keng	1	50.00	-	-	-	-	-	-	-	-	-	-
KAL	-	-	-	-	32,300,000	100.00	-	-	413,000,000	68.49	-	-
AQSB	-	-	-	-	-	-	-	-	133,000,000	22.06	-	-
CTVSB	-	-	-	-	-	-	-	-	57,000,000	9.45	-	-
KAGL	-	-	-	-	-	-	(1)32,300,000	100.00	-	-	(1)413,000,000	68.49
PSL	-	-	-	-	-	-	(1)32,300,000	100.00	-	-	(1)413,000,000	68.49
TCPL	-	-	-	-	-	-	(1)32,300,000	100.00	-	-	(1)413,000,000	68.49
Eg Kah Yee	-	-	-	-	-	-	(2)32,300,000	100.00	-	-	(2)413,000,000	68.49
Chang Tao-Chun	-	-	-	-	-	-	(3)32,300,000	100.00	-	-	(3)413,000,000	68.49
Fang Chun- Jung	-	-	-	-	-	-	(4)32,300,000	100.00	-	-	(4)413,000,000	68.49
Chang Li-Ping	-	-	-	-	-	-	(4)32,300,000	100.00	-	-	(4)413,000,000	68.49
CAVSB	-	-	-	-	-	-	-	-	-	-	(5)57,000,000	9.45
CIMBG	-	-	-	-	-	-	-	-	-	-	(6)57,000,000	9.45
BCHB	-	-	-	-	-	-	-	-	-	-	(7)57,000,000	9.45
Khazanah	-	-	-	-	-	-	-	-	-	-	(8)190,000,000	31.51

Notes:

(1) *Deemed interested by virtue of their interest in KAL pursuant to Section 6A of the Act.*

(2) *Deemed interested by virtue of his interest in KAGL pursuant to Section 6A of the Act.*

(3) *Deemed interested by virtue of his interest in PSL pursuant to Section 6A of the Act.*

(4) *Deemed interested by virtue of their interest in TCPL pursuant to Section 6A of the Act.*

(5) *Deemed interested by virtue of their interest in CTVSB pursuant to Section 6A of the Act.*

(6) *Deemed interested by virtue of their interest in CAVSB pursuant to Section 6A of the Act.*

(7) *Deemed interested by virtue of their interest in CIMBG pursuant to Section 6A of the Act.*

(8) *Deemed interested by virtue of their interest in AQSB and BCHB pursuant to Section 6A of the Act.*

7.3 KEY MANAGEMENT AND TECHINICAL PERSONNEL

The profiles of our key management and technical personnel are set out below.

7.3.1 Profiles

Lai Kok Keong, a Malaysian, aged 38, was appointed as our Chief Executive Officer and acting Director of R&D Department on 1 April 2007. He graduated with a Bachelor of Science degree in Engineering (Computer System) from University of Western Michigan, USA in 1996. He started his career with Intel (M) Technology Sdn Bhd ("Intel") as a Design Automation Engineer in 1996. Since then, he has led multiple IC design projects at Intel including CPU designs of latest IA32 multi-core processor, Pentium 4 and IA32 platform chipset design. He was the leading engineer to develop Intel Pentium chipset and his specialty is in the area of CPU micro-architecture design and optimisation of the design for performance and power. He has published technical papers and won awards in Intel. His last held position in Intel was Senior Manager in CPU Design Division. Subsequently, in 2006, he joined our Group as the R&D Director and was promoted to his current position in 2007.

Loo Kok Weng, a Malaysian, aged 32, was appointed as our Product Engineering Manager on January 2007. He obtained his Bachelor of Electrical Engineering (1st Class Honors) degree from University of Malaya in 1999. He also obtained his Master of Microelectronics Engineering degree from Multimedia University, Malaysia in 2007. He started his career as Material Engineer and Microprocessor Failure Analysis Engineer at Intel. Then, he joined Altera Corporation (M) Sdn Bhd in 2001 as IC Design Engineer in which he led a team of IC engineers in designing I/O Buffer and full-chip power bus. In 2005, he joined Jaalaa Malaysia Sdn Bhd as Project Manager. He was responsible for managing 2 projects for 0.13µ radio frequency IC chip design and development before joining Key ASIC.

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

Lam Che Wai, a Malaysian, aged 31, was appointed as our Lead Technical Design Engineer on 28 March 2006. He obtained his Bachelor of Electrical and Electronic Engineering degree from University of Science Malaysia in 2000. He started his career with Intel Penang Design Centre as Pentium 2 and Pentium 4 chipset design engineer in 2000. He later joined the Intel Pentium 4 CPU design team in 2001, worked in three Pentium 4 CPU design projects from 2001 to 2006. Thereafter, he worked with Intel CPU circuit technology group, mainly on CPU circuit robustness and aging studies. He has jointly disclosed 4 inventions in CPU circuit designs, which one of them has been selected for publication in an Intel-selected technical bulletin for idea protection.

Chan Woo Nam, an American, aged 80, was designated by us as our Vice-President of Strategic Accounts pursuant to a Management Agreement with Key ASIC Inc. dated 1 January 2006. He graduated with a Bachelor of Computer Science degree from Seoul National University, South Korea in 1947. He started his career with Computer Vision Corporation MASS in 1978. He then served as a Country Manager for Daisy for 7 years from 1988. Following that, he became the Managing Director for Asia Pacific Operation with Logic Modelling Corporation in Beaverton, Oregon, USA for 4 years. He was a Senior Vice-President of Strategic Accounts for Cadence Design Systems in Milpitas, California for 2 years and subsequently he worked as a Senior Director, Asia Pacific Operation in Synopsys Inc. for 10 years. After that, he served as the Vice-President of Strategic Accounts with Arcadia Design Systems in Santa Clara, California for a year. Pursuant to a Management Agreement dated 1 January 2006, we have engaged Key ASIC Inc. to sell and market our services. Chan Woo Nam has been appointed by Key ASIC Inc. to act as liaison with our Group and as head of sales, marketing and technical support for our Group to visit prospective customers and engage them to secure business with us.

Tan Eng Hwa, a Malaysian, aged 46, was appointed as our Director of Production on 2 May 2006. He graduated with a Bachelor of Engineering in Electronic degree from University of Malaya in 1986. He started his career in National Semiconductor Sdn Bhd as a Test Engineer in 1986 and was subsequently promoted to Senior Manager for Test Product Engineering and Department Manager for Advance Package Development in 2003 and he left National Semiconductor Sdn Bhd in 2006 as the Director of Business Planning and Sub-Contractor Management Department before joining Key ASIC.

Thong Kooi Pin, a Malaysian, aged 35 was appointed as our Financial Controller on 25 September 2006. He graduated with a professional degree in Association of Chartered Certified Accountants in 1998 and was admitted as a member of the Malaysian Institution of Accountants as a Chartered Accountant in 2005. Further, he obtained his Masters degree in Business Administration majoring in Finance from Universiti Putra Malaysia in 2006. He started his career as an internal auditor in MBF Finance Bhd in 1994 and later joined OUB Finance Bhd in the same year. In 1996, he joined MCL Corporation Berhad (now known as Jerasia Berhad) as Accounts Executive before joining Palette Multimedia Berhad in 1999 as an Accountant. He left Palette Multimedia Berhad in 2003 and subsequently joined M-Mode Berhad as Finance Manager. He was later promoted to Executive Director on 21 September 2005 before joining Key ASIC in 2006. Currently, he sits on the Board of Directors of M-Mode Berhad and Palette Multimedia Berhad as Executive Director and Independent Non-Executive Director respectively.

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

7.3.2 Shareholdings in our Company

The shareholdings of our key management and technical personnel in our Company, before and after the Public Issue are as follows:

		< ----------Before the Public Issue ---------- >				< ---------- After the Public Issue ---------- >			
		<---------Direct---------->		<---------Indirect-------->		<---------Direct---------->		<---------Direct---------->	
	Designation	**No. of Shares**	**%**	**No. of Shares**	**%**	**No. of Shares**	**%**	**No. of Shares**	**%**
Lai Kok Keong	Chief Executive Officer and Acting Director of R&D Department	-	-	-	-	-	-	-	-
Loo Kok Weng	Product Engineer Manager	-	-	-	-	(1)1,800,000	0.22	-	-
Lam Che Wai	Lead Technical Design Engineer	-	-	-	-	(1)1,140,000	0.14	-	-
Chan Woo Nam	Vice President of Strategic Accounts	-	-	-	-	-	-	-	-
Tan Eng Hwa	Director of Production	-	-	-	-	(1)100,000	0.01	-	-
Thong Kooi Pin	Financial Controller	-	-	-	-	(1)3,700,000	0.46	-	-

Note:

(1) Represents the number of Key ASIC Shares allocated pursuant to the pink form portion under the Retail Offering and assuming that the eligible employees will subscribe to Key ASIC Shares in full.

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

7.3.3 Involvement in other Businesses/Corporations

Save as disclosed below, none of our key management and technical personnel is involved in any full-time position in other businesses and/or corporations which would affect their contribution to our Group:

				Substantial shareholdings as at 30 November 2007			
				Direct		Indirect	
Name	Company	Principal activities	Position	No of ordinary shares held	%	No of ordinary shares held	%
Thong Kooi Pin	Palette Multimedia Berhad	Investment holding and design, development and marketing of information technology related products and services.	Independent Non-Executive Director	-	-	-	-
	M-Mode Berhad	Investment holding	Executive Director	130,500	0.90	-	-
	eCentury Sdn Bhd	Provision of mobile contents and data application services	Director	-	-	-	-
	Mobile Multimedia Sdn Bhd	Provision of mobile contents and data application services	Director	-	-	-	-
	M-Mode Technology Sdn Bhd	Provision of mobile contents and data application services	Director	-	-	-	-

Whilst Thong Kooi Pin had interest and/or sits on the board of directors of several companies which are not within our Group, these companies are either involved in investment holdings activities or other business activities which are not in conflict with the business of our Group. His involvement in these companies does not preclude him from allocating a substantial portion of his time in the affairs of our Group where he acts as a Financial Controller because the day-to-day management of these companies are managed by well-qualified and experienced personnel. He only attends meetings of the other board on which he serves and accordingly discharges his principal areas of responsibility as a director in these companies. Although he serves as an Executive Director in M-Mode Berhad, his involvement in the company is on an ad-hoc basis only. His involvement in all these companies is not expected to affect his contribution to our Group.

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

7.4 RELATIONSHIPS AND ASSOCIATIONS

Save as disclosed below, there are no relationships/association among our Directors, substantial shareholders, Promoters and key management:

Company/Director	Relationship/ Association
KAL	Our Company's Director, namely Eg Kah Yee is also a director in KAL.
AQSB	Two (2) of our Company's Directors, namely Eg Kah Yee and Jalaluddin bin Mohd Jarjis are also directors in AQSB. Our Company's Director, Henry Choo Hon Fai is also a key management personnel in AQSB.
Eg Kah Yee	He is a substantial shareholder in KAL, via his shareholding in KAGL. He is also a director and chief executive officer of AQSB and Silterra respectively. He has common directorship with fellow Director, namely Jalaluddin bin Mohd Jarjis in AQSB and Silterra.
Jalaluddin bin Mohd Jarjis	He is a director and chairman in AQSB and Silterra. He has common directorship with fellow Director, namely Eg Kah Yee in AQSB and Silterra.
Henry Choo Hon Fai	He is a key management personnel in AQSB. He is the Chief Operating Officer and Vice-President for Investment in AQSB and Executive Assistant to the Chairman of Silterra respectively.
Lai Yit Loong	He is the Vice-President of Worldwide Sales and Marketing in Silterra. Lai Kok Keong, our key management personnel is the younger brother to Lai Yit Loong.

7.5 DECLARATION BY PROMOTERS, DIRECTORS, KEY MANAGEMENT AND TECHNICAL PERSONNEL

None of our Promoters, Directors and key management personnel is or has been involved in any of the following events (whether in or outside Malaysia):

(i) a petition under any bankruptcy or insolvency laws filed (and not struck out) against such person or any partnership in which he was a partner or any corporation of which he was a director or key personnel;

(ii) disqualified from acting as a director of any corporation, or from taking part directly or indirectly in the management of any corporation;

(iii) charged and/or convicted in a criminal proceeding or is a named subject of a pending criminal proceeding;

(iv) judgment entered involving a breach of any law or regulatory requirement that relates to the securities or futures industry; or

(v) the subject of any order, judgment or ruling of any court, government or regulatory authority or body temporarily enjoining him from engaging in any type of business practice or activity.

7.6 SERVICE AGREEMENTS

Neither we nor our subsidiary has any existing or proposed service agreements with our Directors and/or key management personnel apart from the normal employment contracts with our employees.

7.7 EMPLOYEES

As at 30 November 2007, our Group has a workforce of 23 employees excluding 7 members of the Board of Directors. None of our employees belong to any trade unions and there have been no industrial dispute since we commenced operations. Our management enjoys a cordial relationship with all our employees.

The breakdown of our employees as at 30 November 2007 is as follows:

	<---------- Number of staff ---------->				
Category of employee	**< 6 months**	**1 year**	**> 1 year**	**Total**	**Average years of service**
Managerial and professional	1	2	3	6	1.0
R&D ASIC engineers	6	4	6	16	0.9
R&D product engineers	-	-	-	-	-
Sales & Marketing	-	-	-	-	-
Operations	1	-	-	1	0.1
	8	6	9	23	0.9

Note:

* *There are 2 contract employees in the Company as at 30 November 2007.*

7. INFORMATION ON OUR DIRECTORS, PROMOTERS, SUBSTANTIAL SHAREHOLDERS, KEY MANAGEMENT AND TECHNICAL PERSONNEL *(CONT'D)*

We were incorporated for slightly more than 2 years only. Hence, the average employee serving period is still relatively short as majority of them are serving between 6 months to 1 year period. Our Group has an aggressive human resource plan to hire more engineers to base in the R&D centre in Malaysia. Our Group also places great emphasis in ensuring the continuous training and development of our employees. We focus on providing a structured approach for the training and development of our employees by assessing the capabilities required to implement our business strategies to individual training needs to ensure that the employees have the requisite skills and knowledge.

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